Kindly amend the claims without prejudice, as follows:

Cancel claims 34 and 38-40, without prejudice.

Add claims 46 and 47.(consisting of rewritten allowed claims 39 and 40)

Note that claims 1-29 were previously canceled.

LISTING OF CLAIMS

1. (Previously canceled)
2. (Previously canceled)
3. (Previously canceled)
4. (Previously canceled)
5. (Previously canceled)
6. (Previously canceled)
7. (Previously canceled)
8. (Previously canceled)
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11. (Previously canceled)
12. (Previously canceled)
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18. (Previously canceled)
19. (Previously canceled)
20. (Previously canceled)
21. (Previously canceled)
22. (Previously canceled)
23. (Previously canceled)
24. (Previously canceled)
25. (Previously canceled)

26. (Previously canceled)

27. (Previously canceled)

28. (Previously canceled)

29. (Previously canceled)

30. (Currently amended) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a comparison module receiving output signals from both said write counter and said read counter to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

31. (Previously presented) A dual loop synchronization system as in claim 30, wherein said PLL is embedded within the DLL.

32. (Currently amended) A dual loop synchronization system as in claim 30, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register is a phase detector.

33. (Currently amended) A dual loop synchronization system as in claim 32, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO register is a binary phase detector.

34. (Canceled)

35. (Previously presented) A dual loop synchronization system as in claim 30, wherein said PLL further comprises:

a loop filter coupled between sad PFD and said VCO.

36. (Currently amended) A dual loop synchronization system as in claim 35, wherein the loop filter coupled between ~~sad~~ said PFD and said VCO is configured as a wide bandwidth loop for suppressing VCO phase noise.

37. (Currently amended) A dual loop synchronization system as in claim 30, wherein said digital loop filter coupled between said detector and said phase shifter of said PLL to produce ~~a~~ the phase shift in said ~~PL~~ PLL is a narrow bandwidth filter.

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. (Currently amended) A method for data synchronization in a plesiochronous system comprising the steps of:

receiving write data in a first-in first out (FIFO) register;

detecting the fill level of the FIFO register at the input of a delay locked loop (DLL);

providing a signal based on the detected fill level to a phase lock loop (PLL);

receiving a local reference clock signal in the PLL;

shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL.

42. (Currently amended) A method for data synchronization in a plesiochronous system as in claim ~~40~~ 41, further comprising:

filtering the signal based on the detected fill level in the DLL before providing it to the PLL.

43. (Currently amended) A method for data synchronization in a plesiochronous system as in claim 42, wherein the step of filtering is performed ~~with~~ in a narrow bandwidth filter.

44. (Currently amended) A method for data synchronization in a plesiochronous system as in claim ~~40~~ 41, wherein in the step of receiving a the local reference clock signal in the PLL, the local reference clock is received at a phase/frequency detector in the PLL and further comprising:

filtering a signal at the output of the phase/frequency detector in a loop filter; and

providing the output of the loop filter to a VCO.

45. (Previously presented) A method for data synchronization in a plesiochronous system as in claim 44, wherein the step of filtering is performed in a wide bandwidth filter.

46. (New) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO

configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a reset counter receiving input signals from both said write counter and said read counter;

a register receiving input signals from both said reset counter and said read counter to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

47. (New) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input;

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a binary decoder;

a plurality of phase detectors receiving input signals from both said write counter and said read counter and providing output signals to said binary decoder to generate the fill level; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.